Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A method, comprising:

inputting an input word to a plurality of hash circuits, each hash circuit being responsive to a different portion of said input word;

outputting a hash signal from each hash circuit;

enabling portions of a CAM in response to said hash signals;

inputting said input word to said CAM;

comparing said input word in the enabled portions of said CAM; and

outputting information responsive to said comparing.

2. (previously presented) The method of claim 1 additionally comprising assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of said input word.

3. (previously presented) The method of claim 1 additionally comprising inputting the least significant n bits of said input word to a memory, and wherein said outputting includes selecting between information responsive to a match being found in said memory and information responsive to a match being found in said CAM.

4. (previously presented) The method of claim 1 additionally comprising delaying the inputting of said input word to said CAM until said enabling is completed.

5. (previously presented) The method of claim 1 wherein said enabling includes using said hash signals to select from a plurality of stored signals, and using the selected stored signals to enable a portion of said CAM.

6. (previously presented) The method of claim 5 wherein said using the selected stored signals includes using a starting index and a run length.

7. (previously presented) The method of claim 5 wherein said using the selected stored signals includes using a starting index and an ending index.

8. (previously presented) A method of operating a CAM, comprising:

hashing a comparand word;

precharging certain portions of a CAM in response to said hashing; and

inputting said comparand word to said CAM.

9. (previously presented) The method of claim 8 wherein said hashing includes hashing different n-bit portions of said comparand word.

10. (previously presented) The method of claim 8 additionally comprising inputting the least significant n bits of said comparand word to a memory, and outputting information responsive to one of a match being found in said memory and a match being found in said CAM.

11. (previously presented) The method of claim 8 additionally comprising delaying the inputting of said comparand word to said CAM until said precharging is completed.

12. (previously presented) The method of claim 8 wherein said precharging includes using said hash signals to select from a plurality of stored signals, and using the selected stored signals to precharge portions of said CAM.

13. (previously presented) The method of claim 12 wherein said using the selected stored signals includes using a starting index and a run length.

14. (previously presented) The method of claim 12 wherein said using the selected stored signals includes using a starting index and an ending index.

15. (previously presented) A method of operating a CAM for processing address information, comprising:

inputting an Internet address to a plurality of hash circuits, each hash circuit being responsive to a different portion of said address;

outputting a hash signal from each hash circuit;

using said hash signals to identify portions of a CAM;

inputting said address to said CAM;

comparing said address in only the identified portions of said CAM; and

outputting port information in response to a match being found in said CAM.

16. (previously presented) The method of claim 15 additionally comprising assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of said address.

17. (previously presented) The method of claim 15 additionally comprising inputting the least significant n bits of said address to a memory, and wherein said outputting includes selecting between port information associated with a match in said memory and port information associated with a match in said CAM.

18. (previously presented) The method of claim 15 additionally comprising delaying the inputting of said address to said CAM until portions of said CAM have been precharged in response to said hash signals.

19. (previously presented) The method of claim 15 wherein said using said hash signals includes using said hash signals to select from a plurality of stored signals, and using the selected stored signals to precharge portions of said CAM.

20. (previously presented) The method of claim 19 wherein said using the selected stored signals includes using a starting index and a run length.

21. (previously presented) The method of claim 19 wherein said using the selected stored signals includes using a starting index and an ending index.

22. (previously presented) A method of operating a CAM for processing address information, comprising:

hashing different prefixes within an Internet address;

precharging certain portions of a CAM in response to said hashing;

comparing said Internet address in said precharged portions of the CAM; and

outputting information in response to a match being found in the CAM.

23. (previously presented) The method of claim 22 additionally comprising inputting the least significant n bits of said address to a memory, and wherein said outputting information includes selecting between information associated with a match in said memory and information associated with a match in said CAM.

24. (previously presented) The method of claim 22 additionally comprising delaying said comparing until said precharging is completed.

25. (previously presented) The method of claim 22 wherein said precharging includes using said hash signals to select from a plurality of stored signals, and using the selected stored signals to precharge portions of the CAM.

26. (previously presented) The method of claim 25 wherein said using the selected stored signals includes using a starting index and a run length.

27. (previously presented) The method of claim 25 wherein said using the selected stored signals includes using a starting index and an ending index.

28. (previously presented) A circuit, comprising:

a CAM for receiving a comparand word;

a plurality of hash circuits connected in parallel, each for producing a hash signal in response to a portion of the comparand word; and

a circuit, responsive to said hash signals, for precharging portions of said CAM.

29. (previously presented) The circuit of claim 28 wherein said circuit responsive to said hash signals includes a plurality of memory devices responsive to said hash signals and enable logic responsive to said plurality of memories.

30. (previously presented) The circuit of claim 29 wherein said plurality of memory devices includes a plurality of SRAMs.

31. (previously presented) The circuit of claim 28 additionally comprising an output memory device responsive to said CAM for outputting information in response to a match in said CAM.

32. (previously presented) The circuit of claim 31 additionally comprising an input memory device responsive to a portion of the comparand word, and a switch responsive to said input memory device and said output memory device.

33. (previously presented) The circuit of claim 28 additionally comprising a processor, said CAM, said plurality of hash circuits, and said circuit responsive to said hash circuits receiving information from said processor.

34. (previously presented) A circuit, comprising:

a CAM;

a plurality of hash circuits each for producing a hash signal in response to a portion of a comparand word;

a plurality of memory devices responsive to said hash circuits;

enable logic, responsive to said plurality of memory devices, for enabling portions of said CAM; and

a delay circuit for inputting the comparand word to said CAM.

35. (previously presented) The circuit of claim 34 wherein said plurality of memory devices includes a plurality of SRAMs.

36. (previously presented) The circuit of claim 34 additionally comprising an output memory device responsive to said CAM for outputting information in response to a match in said CAM.

37. (previously presented) The circuit of claim 36 additionally comprising an input memory device responsive to a portion of the comparand word, and a switch responsive to said input memory device and said output memory device.

38. (previously presented) The circuit of claim 34 additionally comprising a processor for initializing said hash circuits, said plurality of memory devices and said CAM.

39. - 40. (Cancelled)

41. (currently amended) A method of initializing hardware having a CAM divided into a plurality of banks, said method comprising:

transferring network addresses to a the CAM based on an index to a hash table;

transferring port numbers to an output memory device responsive to the CAM;

modifying bit prefix values to obtain a ternary representation;

calculating bank run length information; and

loading bank starting address and bank run length information into a plurality of memory devices.

42. (previously presented) The method of claim 41 additionally comprising periodically transferring invalid network addresses to the CAM.

43. (previously presented) The method of claim 41 additionally comprising transferring port

information to an SRAM for prefixes below a certain length.

44. (currently amended) The method of claim 41 wherein said bank run length information includes one of ~~an~~ a bank end address and ~~an~~ a bank address span.

Amendments to the Drawings

The attached replacement sheets of drawings include changes to FIG.1, FIG. 2, and FIG. 3 to add legends to certain of the boxes shown in the figures.

Attachments: Replacement sheets 1/5, 2/5, and 3/5
Annotated sheets 1/5, 2/5, and 3/5 showing the changes in red